A High Gain Low Noise 110 GHz Monolithic Two-stage Amplifier

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ABSTRACT

A high gain low noise 110 GHz monolithic two-stage amplifier using 0.1 μm pseudomorphic AlGaAs/InGaAs/GaAs low noise HEMT technology is presented in this paper. This amplifier demonstrates a small signal gain of 19.6 dB at 110 GHz with a noise figure of 3.9 dB. A noise figure of 3.4 dB with 15.6 dB associated gain was obtained at 113 GHz. The small signal gain and noise figure performance are the best results ever achieved for a two-stage HEMT amplifier at these frequencies.

INTRODUCTION

Monolithic millimeter-wave (MMW) integrated circuits provide significant advantages of high reliability, light weight, small size and low cost for high volume production over conventional hybrid circuits in MMW radar, smart munitions, and radiometric system applications. Low noise amplifier (LNA) is an important component in the receiving chain of these systems. Therefore there is a need to pursue the development of MMW monolithic LNA for future low cost system applications.

The pseudomorphic (PM) HEMT devices using both GaAs and InP based technologies have demonstrated high gain and low noise capabilities at W-band frequency and higher for hybrid integrated circuits [1]-[3]. Although InP based discrete HEMT devices show better performance at W-band and higher frequencies [2]-[3], GaAs based HEMT MMIC technology offers superior design and process maturity compared with InP based HEMT MMIC technology. High gain, low noise 94 GHz monolithic LNAs have been successfully developed using PM AlGaAs/InGaAs/GaAs HEMT devices [4]-[6]. The motivation of this work is pushing forward higher frequency performance of the monolithic LNAs using the developed device technology [1], [4]-[6] to enable new system applications. A monolithic two-stage LNA with 12 dB gain and 6.3 dB noise figure at 113 GHz was first reported [7]. This paper presents another design of monolithic LNA at this frequency using the same device technology, which demonstrates a gain of 19.6 dB at 110 GHz with a noise figure of 3.9 dB. A noise figure of 3.4 dB with 15.6 dB associated gain was obtained at 113 GHz. The small signal gain and noise figure performance are the best results ever achieved for a two-stage HEMT amplifier at this frequency.

DEVICE CHARACTERISTICS AND MODELING

The HEMT devices used in the LNA design have been optimized for high gain operation at W-band. The 22% In PM AlGaAs/InGaAs/GaAs HEMT uses planar doping to achieve high channel aspect ratio as well as higher electron transfer efficiency. The HEMT device structure and MMIC fabrication process used for this work has been previously reported [1],[4]. The 0.1 μm T-gate HEMTs fabricated using this process typically have a dc transconductance (G_m) of 670 mS/mm with an unit current gain frequency (f_T) of 140 GHz.

The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal S-parameters to 40 GHz. Noise model parameters used for simulation are obtained from fitting measured noise parameters to 26 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters. The details of this modeling procedure were documented in [4].

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CIRCUIT DESIGN

Fig. 1 shows the monolithic LNA circuit shematic diagram and chip photograph. The size of the chip is 2.1 × 1.5 mm^2. Each stage utilizes a 40 μm HEMT with four gate fingers. The input and interstage matching networks are designed for low noise figure and realized by cascade high-low impedance microstrip lines on 100 μm thick GaAs substrate. Edge coupled lines are used for dc block and radial stubs are employed for RF bypass. N^+ bulk resistors and by-pass metal-insulator-metal (MIM) capacitors are used to ensure bias network stability, and reactive ion etching (RIE) process is used to fabricate back side via holes for grounding. The overall circuit design is similar to the previously published W-band monolithic LNAs [4]-[6]. This circuit presented in this paper is designed for high gain and low noise figure, and demonstrates better gain and noise performance than the one reported in [7]. This is because the amplifier reported in [7] utilized a HEMT device layout which was optimized for power performance and the circuit was designed based on the power device model, but the chip was fabricated with low noise HEMT process.

A design procedure using full-wave EM analysis [8] for the passive structures to eliminate the uncertainties due to quasi-static models was incorporated in this 110 GHz monolithic LNA development. The design/analysis methodology was previously described in [4].

CIRCUIT MEASUREMENT

The 110 GHZ monolithic LNA was assembled in a WR6 D-band (110-170 GHz) waveguide test-fixture for measurement. Antipodal finline transitions on 75 μm thick fused silica substrate are used to couple the signal from the waveguide to microstrip. The typical insertion loss of this transition fixture with a back-to-back transition connections is 2 dB with 14 dB return loss.

The LNA circuit was tested at the National Radio Astronomy Observatory (NRAO). The small signal transducer gain was measured by using a scalar network analyzer with a backward wave oscillator (BWO) as a signal source. The noise figure were measured using measurement system described in Fig. 2. The hot (297 K) and cold (77 K) loads are first used for the noise measurement of the receiver (isolator + Schottky diode mixer + IF amplifier) and then for the measurement of the amplifier receiver cascade.

Fig. 3 plots the measured noise figure and associated small signal gain of the LNA from 110 to 115 GHz. All the data shown in the plot have

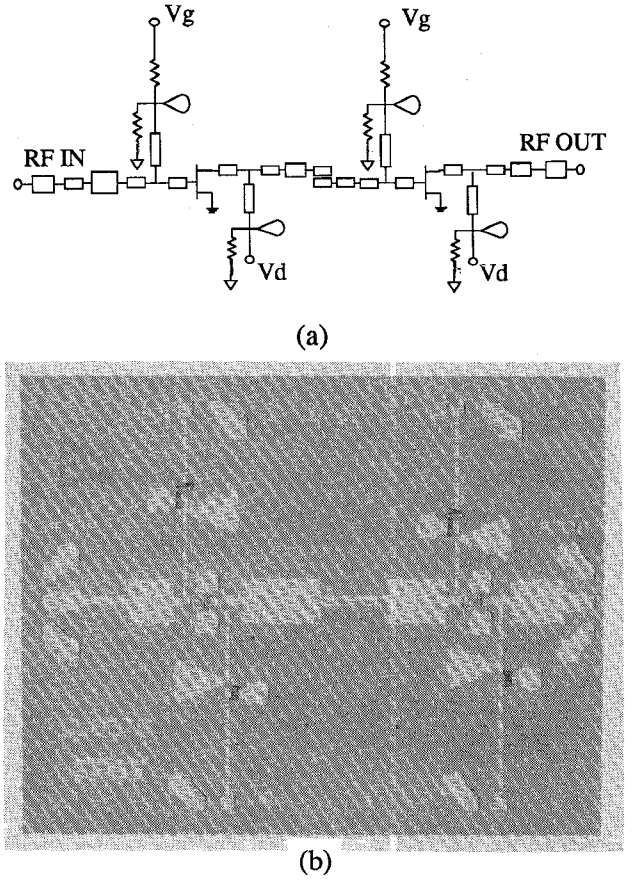

Fig. 1. (a) Circuit schematic diagram, and (b) photograph of the monolithic 110 GHz two-stage LNA.

been corrected by assuming a single side waveguide-to-microstrip finline transition loss of 0.8 dB. During the testing, there was no tuning on the matching structures. The small signal gain is 19.6 dB at 110 GHz. This is the highest gain ever achieved by a two-stage HEMT amplifier in this frequency. The best noise figure point is at 113 GHz which presents a noise figure of 3.4 dB and an associated gain of 15.6 dB. Over the frequency from 110 to 115 GHz, the gain is higher than 12 dB and noise figure is better than 4.3 dB. The results were taken under the bias at 2.7 V drain voltage with each stage taking 32 mA current. Part of the current is consumed by the shunt resistors in the bias networks.

SUMMARY

We have demonstrated a 110 GHz MMIC two-stage LNA with state-of-the-art performance. At 110 GHz, a small signal gain of 19.6 dB and a noise figure of 3.9 dB was achieved. A noise figure of 3.4 dB was obtained at 113 GHz. The

superior results of this monolithic LNA enable system applications at this frequency, such as radiometers and low noise receivers.

ACKNOWLEDGMENT

This work is supported by TRW internal R&D funds. The authors would like to thank Drs. T. H. Chen, K. W. Chang, and B. Allen for their helpful technical discussions and suggestions, G. Coakley for his layout support, R. Dia for wafer processing, the MBE and EBL groups in TRW for their excellent support, D. Garske for her assembly of the chip.

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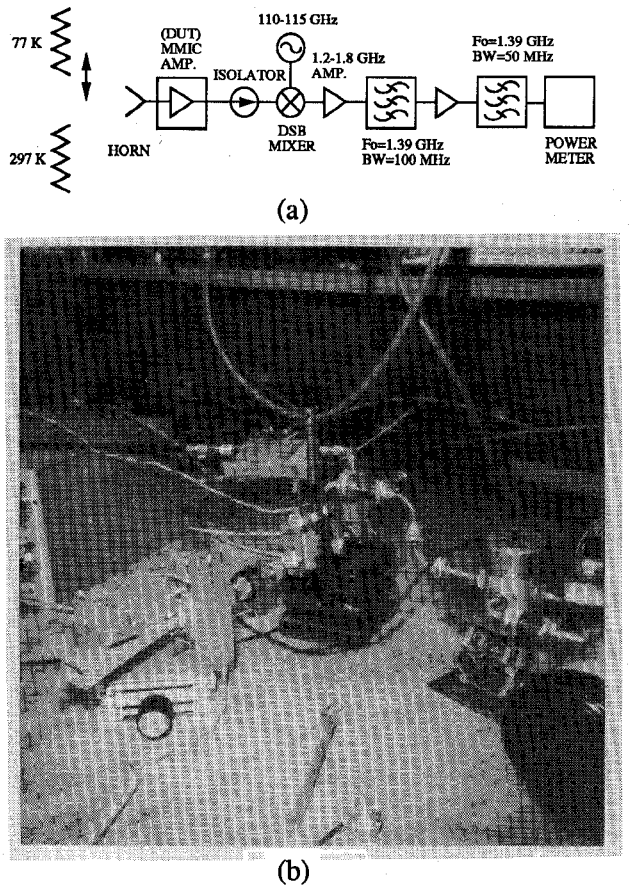

Fig. 2. (a) Block diagram, and (b) photograph of the noise figure measurement setup.

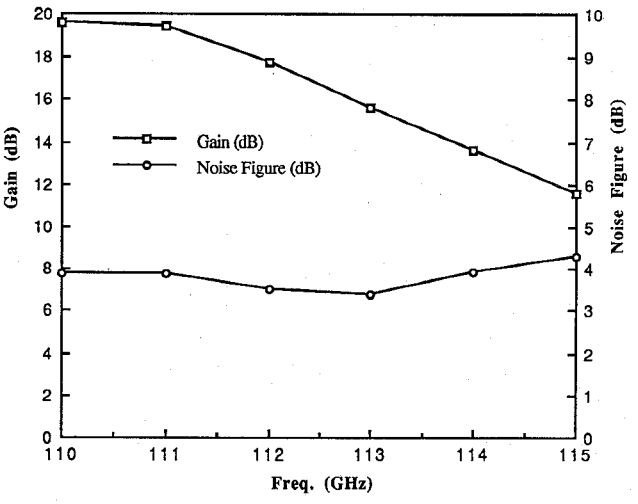

Fig. 3. Measured noise figure and small signal transducer gain of the monolithic D-band two-stage LNA.